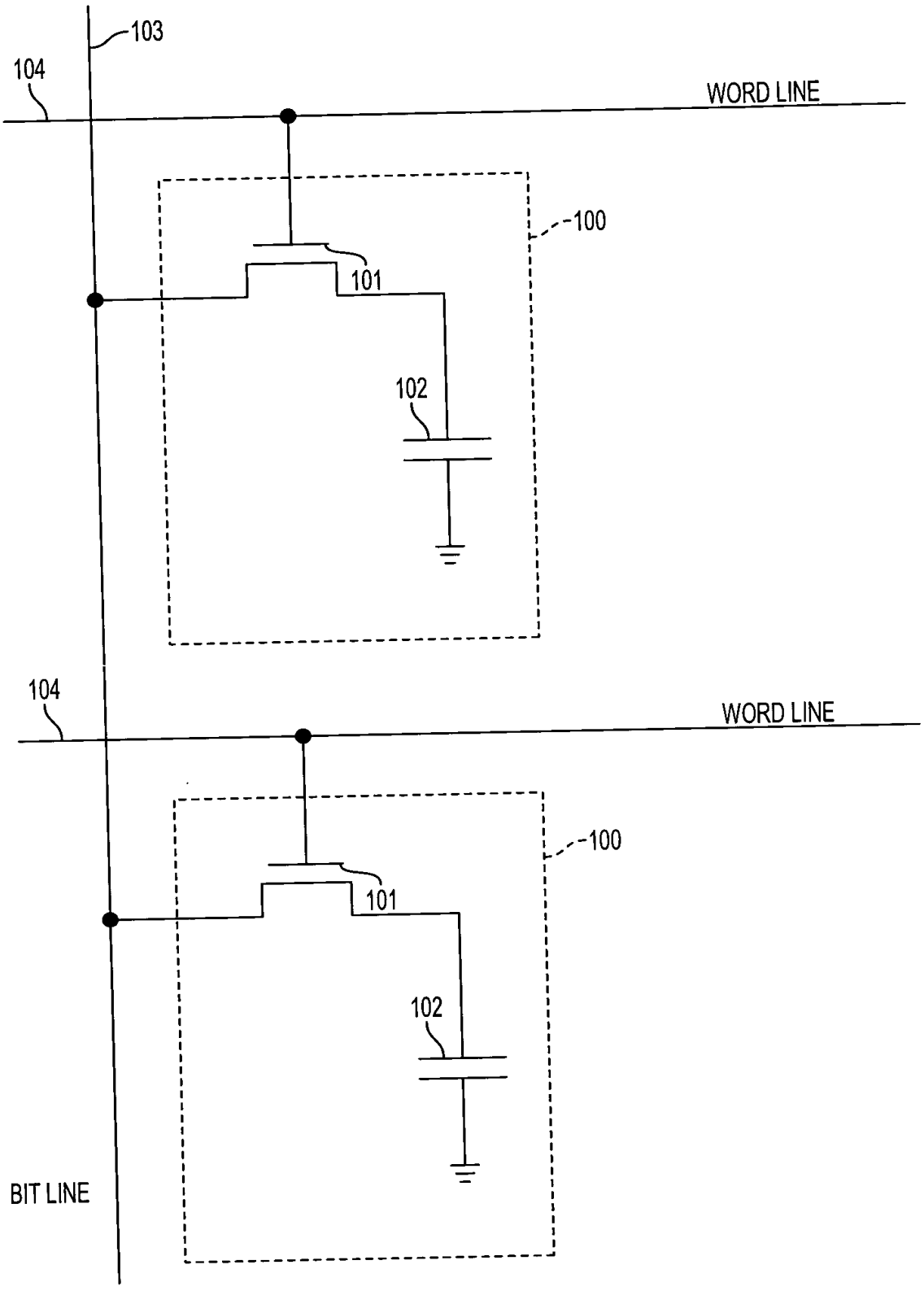

FIG. 1
(PRIOR ART)

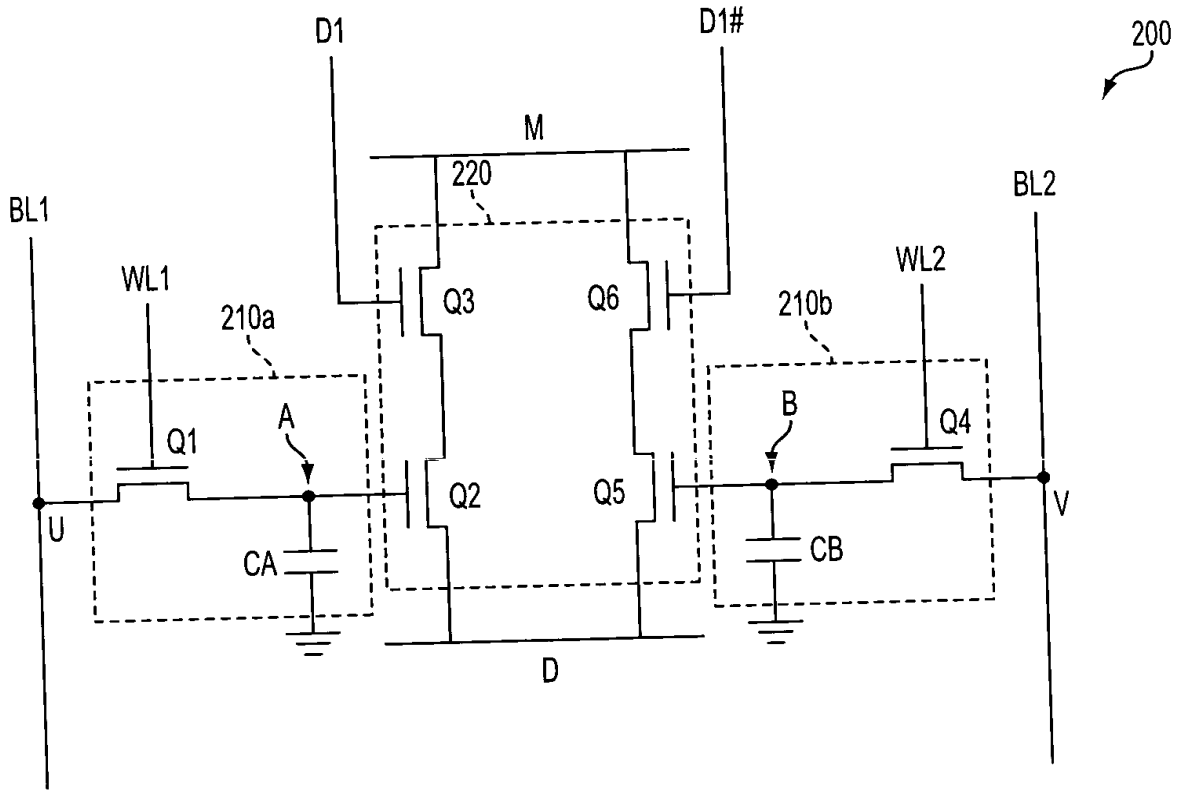

FIG. 2
(PRIOR ART)

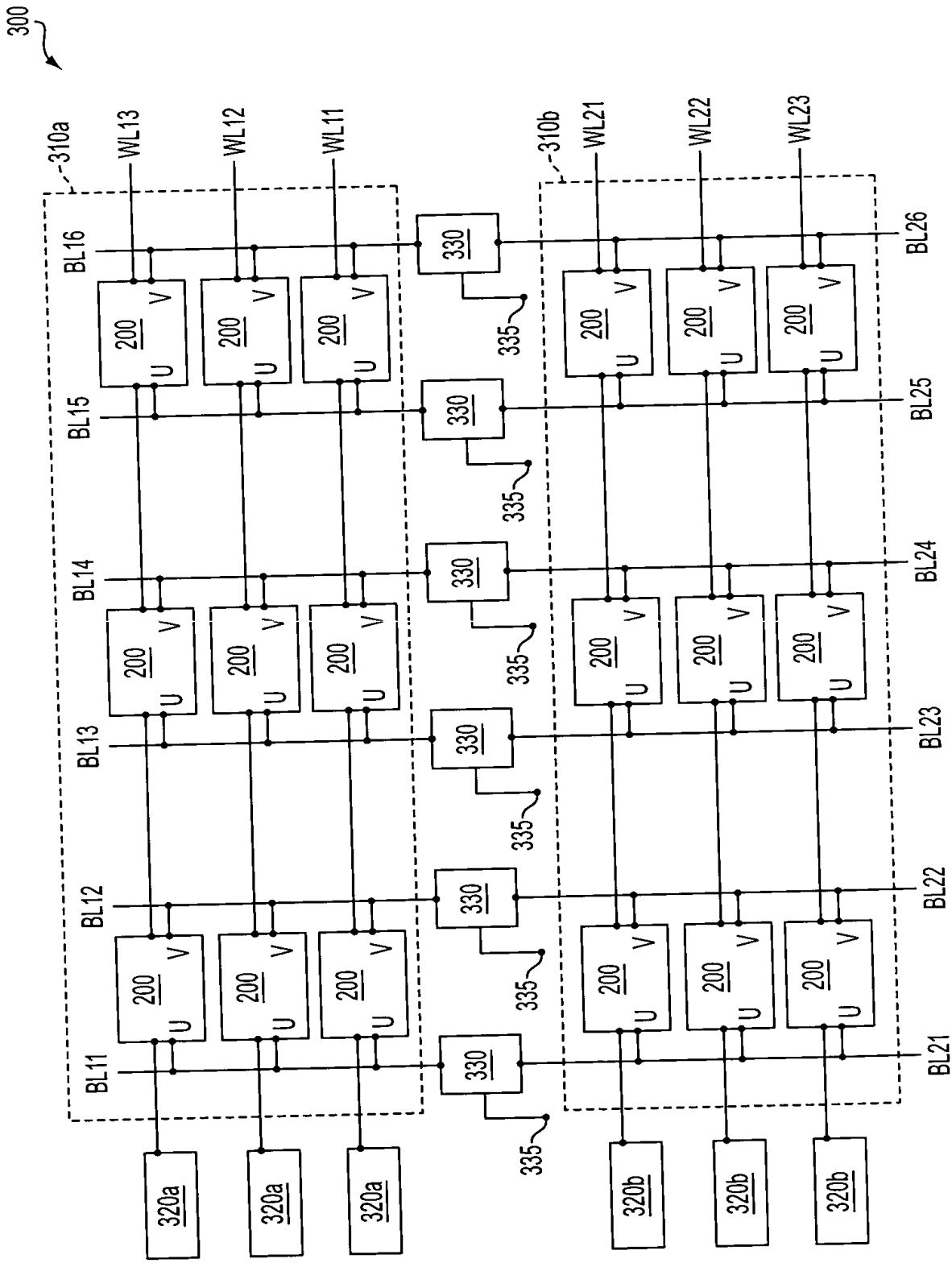

FIG. 3
(PRIOR ART)

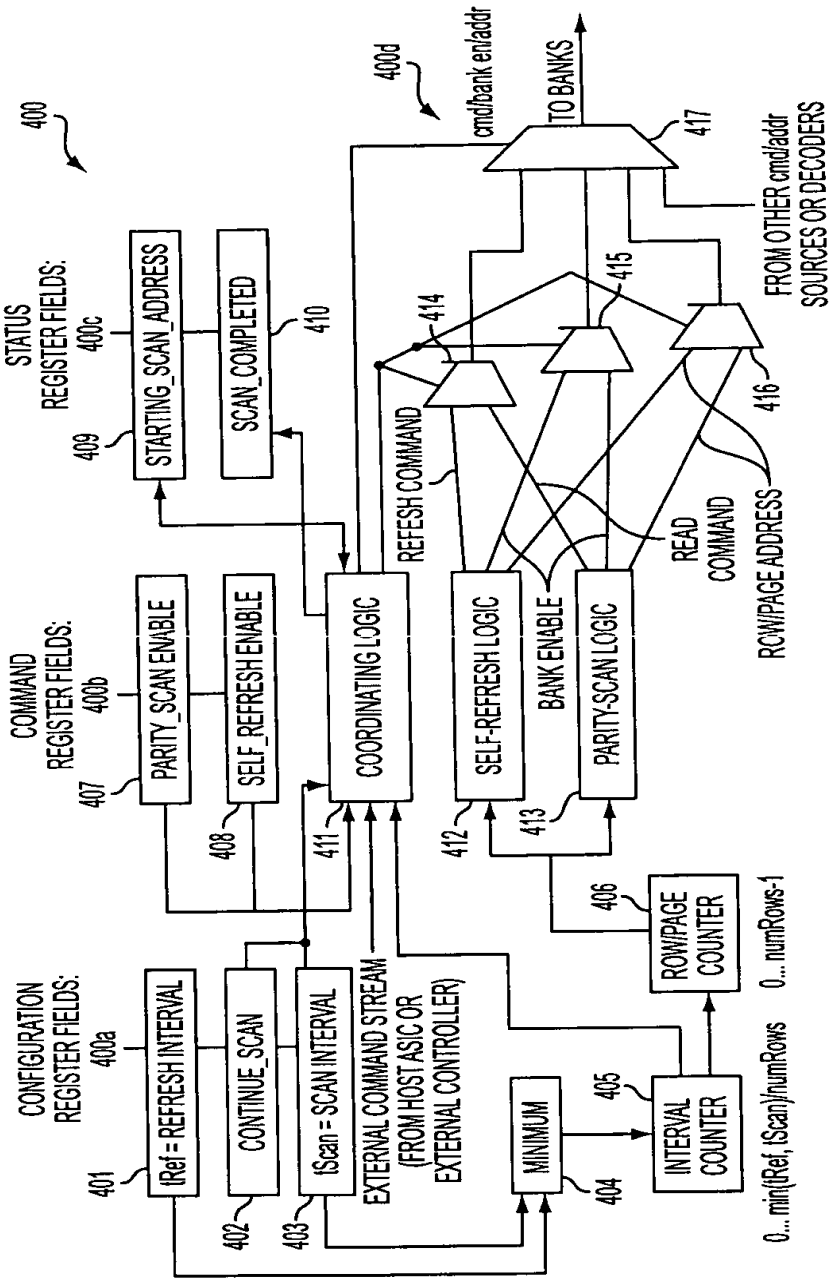
400
CONFIGURATION REGISTER FIELDS:
400a
401
tRef = REFRESH INTERVAL
402
CONTINUE_SCAN
403
tScan = SCAN INTERVAL
EXTERNAL COMMAND STREAM (FROM HOST ASIC OR EXTERNAL CONTROLLER)
MINIMUM
404
405
INTERVAL COUNTER
0... min(tRef, tScan)/numRows
406
ROW/PAGE COUNTER
0... numRows-1
COMMAND REGISTER FIELDS:
400b
407
PARITY_SCAN ENABLE
408
SELF_REFRESH ENABLE
411
COORDINATING LOGIC
412
SELF-REFRESH LOGIC
413
PARITY-SCAN LOGIC
BANK ENABLE
REFESH COMMAND
414
415
READ COMMAND
416
ROW/PAGE ADDRESS
400d
cmd/bank en/addr
TO BANKS
417
FROM OTHER cmd/addr SOURCES OR DECODERS
STATUS REGISTER FIELDS:
400c
409
STARTING_SCAN_ADDRESS
SCAN_COMPLETED
410

FIG. 4

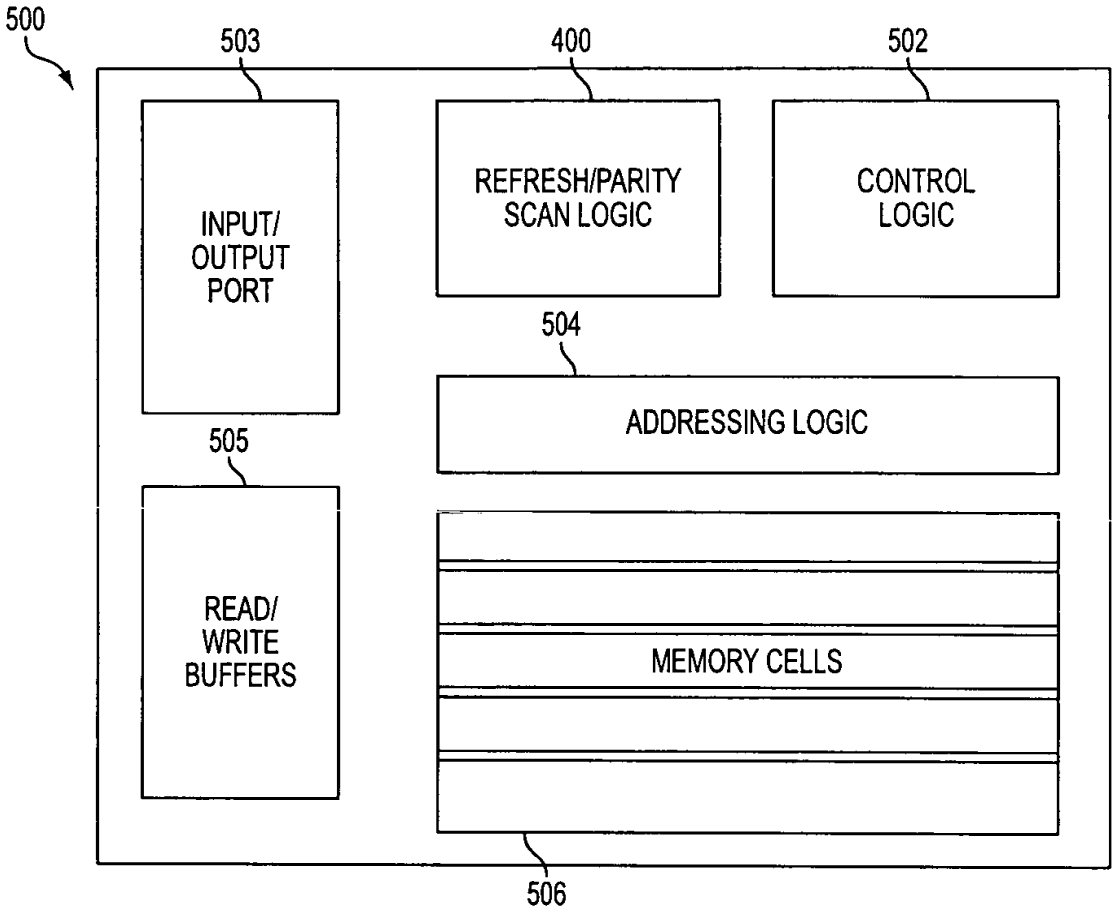
500
503
400
502
INPUT/
OUTPUT
PORT
REFRESH/PARITY
SCAN LOGIC
CONTROL
LOGIC
504
ADDRESSING LOGIC
505
READ/
WRITE
BUFFERS
MEMORY CELLS
506

FIG. 5

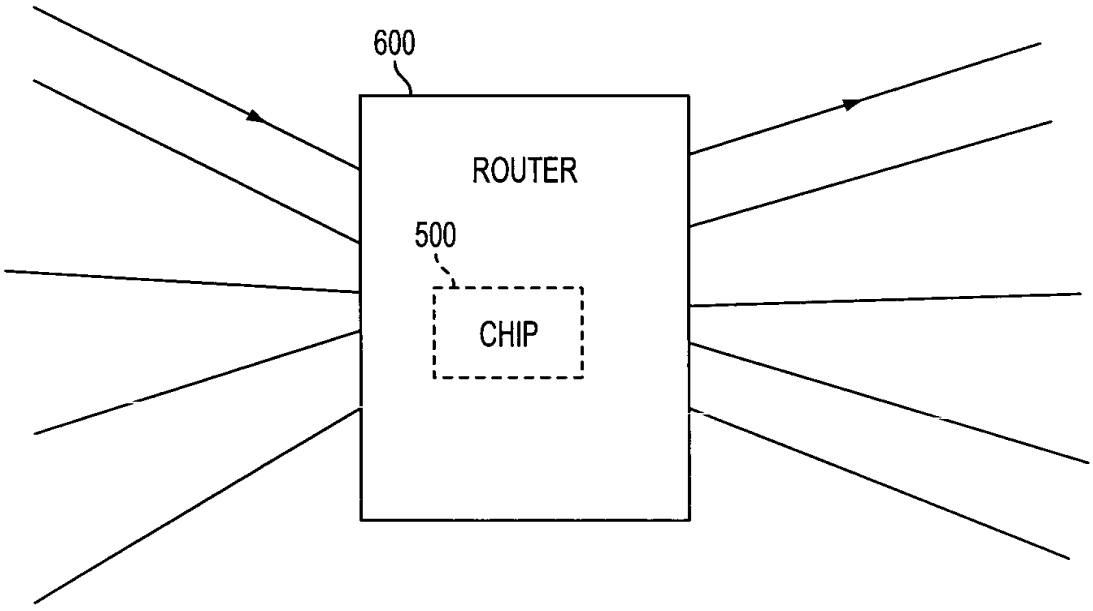

FIG. 6

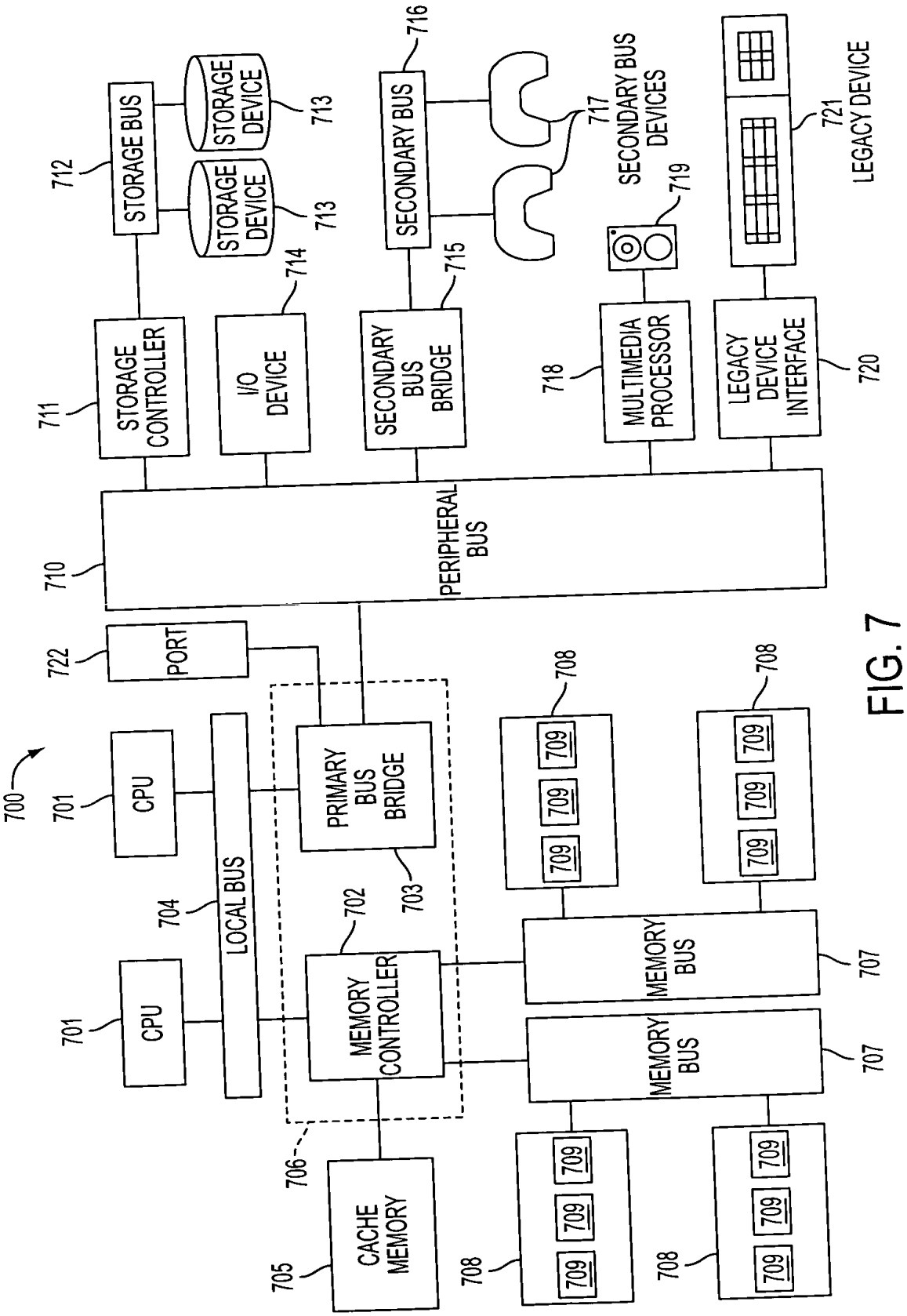
700
701
CPU
701
CPU
704
LOCAL BUS
PRIMARY BUS BRIDGE
703
702
MEMORY CONTROLLER
706
CACHE MEMORY
705
722
PORT
710
PERIPHERAL BUS
711
STORAGE CONTROLLER
712
STORAGE BUS
STORAGE DEVICE
713
STORAGE DEVICE
713
714
I/O DEVICE
715
SECONDARY BUS BRIDGE
716
SECONDARY BUS
717
SECONDARY BUS DEVICES
718
MULTIMEDIA PROCESSOR
719
720
LEGACY DEVICE INTERFACE
721
LEGACY DEVICE
MEMORY BUS
707
MEMORY BUS
707
708
709
708
709
708
709
708
709

FIG. 7